Datasheet

DS000501

NanEye / NanEye Stereo

Miniature Camera Module

v2-02 • 2018-Oct-05

Content Guide

1 General Description

NanEye is a miniature sized image sensor vision applications where size is a critical factor. The ability of the camera head to drive a signal through long cables makes this the ideal component for minimal diameter endoscopes.

With a footprint of a just 1mmx1mm, it features a 249x250 resolution with a high sensitive 3-micron rolling shutter pixel, with large full well capacitance. The sensor has been specially designed for medical endoscopic applications where high SNR is mandatory. The sensor has a high frame rate of about 43 to 62fps to permit SNR enhancement and a smooth, low delay display over a wide range of standard interfaces.

The sensor includes a 10bit ADC and a bit serial LVDS data interface. The sensor is able to drive the signal through a cable length of up to 3m.

The data line is semi duplex, such that configuration can be communicated to the sensor in the frame brake.

The exposure time, dark level and analogue gain can be programmed over the serial configuration interface.

1.1 Key Benefits & Features

The benefits and features of NanEye / NanEye Stereo, Miniature Camera Module, are listed below:

Figure 1:
Added Value of Using NanEye / NanEye Stereo

Benefits	Features
Designed for the toughest confined space requirements	Footprint of 1x1mm with 4 contact pads
Compact stereo vision	Combination of 2 NanEye in 2.2x1mm module
Smooth and accurate image	Frame rate of 43-62fps @ 249x250 resolution
Reach further	Possible to drive a signal through an endoscope of up to 3m
Affordable single use application	Designed with a focus on cost efficiency
Envision the unseen	3-micron high sensitive pixel with 62k pixel resolution (125k for stereo module)

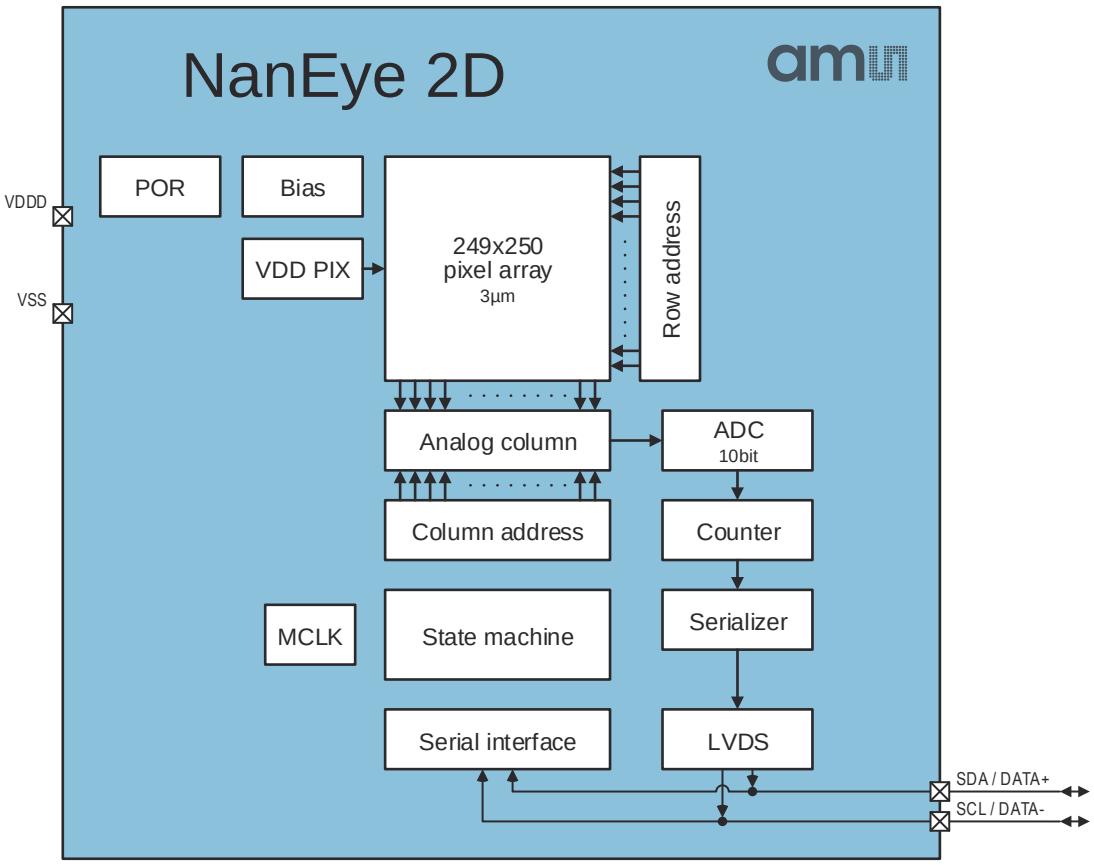
1.2 Applications

- Medical Applications
  - Endoscopy
  - Intraoral Scanning
- Industrial Applications
  - Industrial endoscopy
  - Robotics
  - IoT (Internet of Things)
- Wearable Devices
  - Eye tracking
  - Virtual / Augmented reality
  - Gesture recognition

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of NanEye / NanEye Stereo



2 Ordering Information

Ordering Code	Package	Optics	Delivery Form	Delivery Quantity
CHIP only version				
NE2D_CHIP_B&W_SGA	SGA	No lens	Tray	
NE2D_CHIP_RGB_SGA	SGA	No lens	Tray	
NE2D_B&W_2m	Chip with cable	No lens	Spool	
NE2D_RGB_NP_2m	Chip with cable	No lens	Spool	
B&W version				
NE2D_B&W_FOV90F2.7_2m	Module with cable	FOV90°; F2.7	Spool	
NE2D_B&W_FOV90F4.0_2m	Module with cable	FOV90°; F4.0	Spool	
NE2D_B&W_FOV120F2.8_2m	Module with cable	FOV120°; F2.8	Spool	
NE2D_B&W_FOV120F4.0_2m	Module with cable	FOV120°; F4.0	Spool	
NE2D_B&W_FOV160F2.4_2m	Module with cable	FOV160°; F2.4	Spool	
NE2D_B&W_FOV90F4.0_SGA	Module only	FOV90°; F4.0	Tray	
NE2D_B&W_FOV90F2.7_SGA	Module only	FOV90°; F2.7	Tray	
NE2D_B&W_FOV120F2.8_SGA	Module only	FOV120°; F2.8	Tray	
RGB version				
NE2D_RGB_FOV90F2.7_2m	Module with cable	FOV90°; F2.7	Spool	
NE2D_RGB_FOV90F4.0_2m	Module with cable	FOV90°; F4.0	Spool	
NE2D_RGB_FOV90F6.0_2m	Module with cable	FOV90°; F6.0	Spool	
NE2D_RGB_FOV120F2.8_2m	Module with cable	FOV120°; F2.8	Spool	
NE2D_RGB_FOV120F4.0_2m	Module with cable	FOV120°; F4.0	Spool	
NE2D_RGB_FOV160F2.4_2m	Module with cable	FOV160°; F2.4	Spool	

Ordering Code	Package	Optics	Delivery Form	Delivery Quantity
NE2D_RGB_FOV90F4.0_SGA	Module only	FOV90°; F4.0	Tray	
NE2D_RGB_FOV90F2.7_SGA	Module only	FOV90°; F2.7	Tray	
NE2D_RGB_FOV120F2.8_SGA	Module only	FOV120°; F4.0	Tray	
STEREO view version				
NE2D_RGB_FOV90_F2.7_Stereo_2m	Module with cable	FOV90°; F2.7	Spool	
LED ring version				
NE2D_RGB_FOV90F2.7_LED	Module with cable	FOV90°; F2.7	Spool	

Information

As module the device is mounted on a flat ribbon cable measuring up to 2m in length that connects to the base station. However, if the customer requirements are discussed, it may be possible to assemble a slightly longer cable (up to 3m).

CAUTION

The NanEye Module and NanEye Stereo Module system is NOT supplied sterile! Medical use of the system, not integrated into a medical device, may lead to serious harm, illness or death!

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
Pin Assignment SGA (top view)

	1	2
A	VDDD	SDA / DATA+
B	VSS	SCL / DATA-

Figure 4:
Pin Assignment Module Cable (camera front view)

	1	2	3	4	5	6
4-wire cable	VSS	SDA / DATA+	SCL / DATA-	VDDD		
6-wire cable	LED-	VSS	SDA / DATA+	SCL / DATA-	VDDD	LED+

Figure 5:
4-Wire Cable Pinout

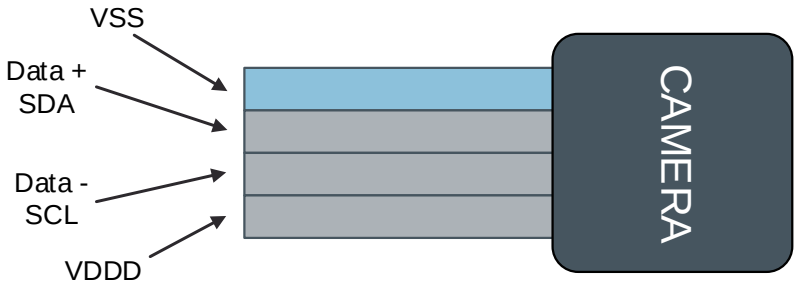
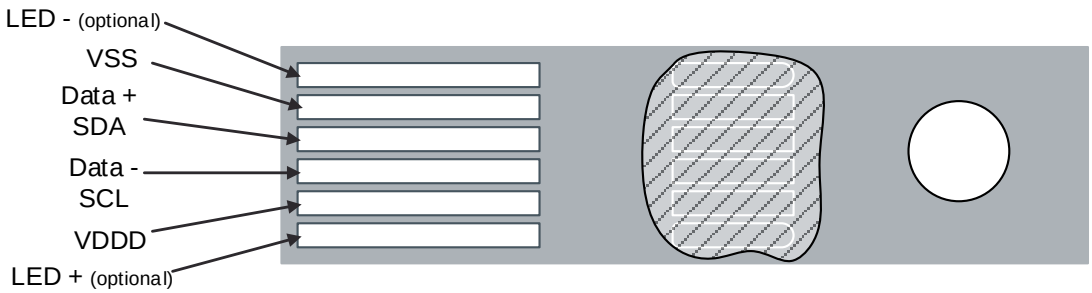


Figure 6:
6-Wire Cable FlexPCB Connector Pinout



3.2 Pin Description

Figure 7:
Pin Description of NanEye / NanEye Stereo

Pin Number			Pin Name	Pin Type(1)	Description
SGA	Cable 4-wire	Cable 6-wire			
		1	LED-	AO	LED cathode
B1	1	2	VSS	VSS	Ground supply
A2	2	3	SDA / DATA+	DIO	Serial data input, LVDS pos. output
B2	3	4	SCL / DATA-	DIO	Serial clock input, LVDS neg. output
A1	4	5	VDDD	Supply	Positive supply
		6	LED+	AI	LED anode

(1) Explanation of abbreviations:
DIO Digital Input/Output
AI Analog Input
AO Analog Output

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings“ may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 8:
Absolute Maximum Ratings of NanEye / NanEye Stereo

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{VDDD}	Supply Voltage to Ground	-0.5	3	V	
V_{SCL}, V_{SDA}	Input Pin Voltage to Ground	-0.5	3	V	
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM		± 1	kV	JEDEC JESD22-A114F
Temperature Ranges					
T_A	Operating Ambient Temperature	-20	60(1)	°C	
T_{100C}	Max Time around 100°C(2)		2	min	
T_{150C}	Max Time around 150°C		10	sec	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020(3)
	Number of reflow cycles		1		Due to the small pad pitch, standard reflow process may need to be adjusted to achieve reliable solder result.
Storage Conditions					
T_{STRG}	Storage Temperature Range	-	30	°C	
R_{HNC_STRG}	Long term storage humidity	-	60	%	
	Shelf life	-	2	year	
MSL Level					
$MSL_{\_SGA}$	Moisture Sensitivity Level SGA without lenses		1		Represents an unlimited floor life time
$MSL_{\_MODULE}$	Moisture Sensitivity Level Lens Module		2(4)		Represents a floor life time of 1 year
$MSL_{\_M+CABLE}$	Moisture Sensitivity Level Lens Module with Cable		N/A		Not applicable as only the cable gets soldered not the module

(1) NanEye can withstand temperatures of 80˚C with no loss of communication. The only change on its performance it’s the slight increase on the dark current/noise, which is normal for high temperatures.
(2) UV curing process is in our conviction not causing any harm to the sensor.
(3) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.” The lead finish is tin/silver (96,5% Sn, 3.5% Ag).
(4) NanEye is not shipped in a moisture barrier package. If soldering is needed a dry bake needs to be performed upfront.

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 9:
Electrical Characteristics of NanEye / NanEye Stereo

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDD	Supply Voltage		(1.6[1])1.8	2.1	2.4	V
$VN_{RMS}VDDD$	RMS noise on VDDD				5	mV
$VN_{PP}VDDD$	Peak to peak noise on VDDD				20	mV
P_{CLK}	Internal pixel clock (adjustable via VDDD)			2.8		MHz
B_{CLK}	Bit clock for serial data transmission (12x Pclk)		30	33.6	46	MHz
J_{DATA}	Jitter data clock		-20		20	% of B_{CLK}
$P_{tot\_1.6}$	Total power consumption	VDDD=1.6V[1]	1.5	3.1	4,7	mW
$P_{tot\_1.7}$	Total power consumption	VDDD=1.7V[1]	2,0	3,8	5,5	mW
$P_{tot\_1.8}$	Total power consumption	VDDD=1.8V	2,6	4,6	6,7	mW
$P_{tot\_2.1}$	Total power consumption	VDDD=2.1V	4,6	7,5	10,5	mW
$P_{tot\_2.4}$	Total power consumption	VDDD=2.4V	6,8	11,5	16,1	mW
Digital Upstream Interface						
V_{IL}	SCL,SDA Low Level input voltage		-0.3		0.22*VDDD	V
V_{IH}	SCL,SDA High Level input voltage		0.71*VDDD		VDDD+0.3	V
T_S	Setup time for upstream configuration relative to SCL		3			ns
T_H	Hold time for upstream configuration relative to SCL		3			ns
f_{SCL}	SCL frequency				2.5	MHz
LVDS Downstream Interface						
V_{CM}	Common mode output voltage (DATA+/-)		0.4	VDDD/2	VDDD-0.4	V
$I_{DATA+,DATA-}$	LVDS output signal current		300	500	600	µA
	Data line impedance	recommended		120		Ω
	LVDS differential peak-peak swing	120Ω		60		mV
$T_{slew,\ rising}$	Output slew rate of rising edge			3		ns
$T_{slew,\ falling}$	Output slew rate of falling edge			3		ns

(1) The frame rate is dependent on VDD sensor supply voltage. For as long as the frame rate is maintained >38 Fps the sensor supply can be set lower than 1.8V down to 1.6V minimum.

Figure 10:
Electro-Optical Characteristics of NanEye / NanEye Stereo

Parameter	Value	Remark
Resolution	62kP, 249 (H) x 250(V)	
Pixel size	3µm x 3µm	
Optical format	1/16"	
Pixel type	3T FSI	
Shutter type	Rolling Shutter	
Color filters	RGB (Bayer Pattern) or B&W	
Micro lenses	no	
Programmable register	Sensor parameter	exposure time, dark level and analog gain
Programmable gain	4 steps -1.5/1/2.4/6.5dB	analog
Exposure times	0.07 – 25 ms	Register configurable
Number of defect pixel(1)	<10	
Defect pixel cluster(2)	0	
ADC	10bit	Column ADC
Frame rate	43-62fps	Adjustable over power supply
Output interface	1x LVDS @ 38Mbps	@50Hz
Size	1 x 1mm -10µm/+30µm	

(1) A pixel is considered a defect pixel if in dark or at any homogeneous illumination level its value deviates more than 200DN with the settings of INVERSE_GAIN= 1, OFFSET=3, VRST_PIXEL = 1, VREF_CDS = 2 rows in reset = 1, VDDD = 2.1V from the median value of it's 8 nearest neighbors. (In case of RGB color sensors, the nearest neighbors are considered from each color plane individually).
(2) A defect pixel cluster is any region of 5 x 5 pixels, which contains more than 1 defect pixel.
(3) Edge chirp of up to 100um from edge of chip package is allowed.
(4) Surface scratch and dig up to 200um length when width above 20um, or of width less than 20um is allowed, for as long as PRNU and defect pixel specification under normal incident illumination and F# 8 is respected.

Figure 11:
Electro-Optical Parameter of NanEye / NanEye Stereo[1][2]

Parameter	Gain=0	Gain=1	Gain=2	Gain=3	Unit
Gain Value	-1.6	1	2.4	6.5	dB
Responsivity	4.6	5.5	7.2	11.5	DN/nJ/cm^2
Full well capacity	17	15.8	13.5	6.8	ke-
QE	30	30	30	30	%
Temporal read noise in dark / dark noise	1	1.1	1.6	2.6	DN
Dynamic Range	56	58	53	49	dB
SNR max	44	41	40	38	dB
DSNU	2.8	3.5	4.7	7	DN
PRNU	5.0	4.8	5.0	5.2	%
FSD	655	890	834	808	DN

(1) Measured on a B&W sensor at 625nm illumination The values are all without software correction and were all measured using the following test equipment: http://www.aphesa.com/EMVA1288_setup.php.

(2) The settings used to get these values are those recommended by the European Machine Vision Association standard 1288 for the Machine Vision Sensors and Cameras: http://www.emva.org/standards-technology/emva-1288/.

Figure 12:
Lens Configuration

Parameter	F#2.7 FOV90º	F#4.0 FOV90º	F#6.0 FOV90º	F#2.8 FOV120º	F#4.0 FOV120º	F#2.4 FOV160º
F# number	2.7	4.0	6.0	2.8	4.0	2.4
FOV (diagonal in air)	90°(1)	90°	90°	120°	120°	160°
FOV (diagonal in water)	62°(1)	62°	62°	86°	86°	95°
Max distortion (diagonal in air)	23%	23%	23%	50%	50%	80%
Max distortion (diagonal in water)	7.5%	7.5%	7.5%	16%	16%	20%
EFL (mm)	0.66	0.66	0.66	0.5	0.5	0.45
Aperture (um)	220	176	120	176	120	180
MTF @ ½ Nyquist @ center (simulated)	69%	73%	65%	66%	73%	57%
MTF @ ½ Nyquist @ 50% diagonal filed Tangential (simulated)	47%	51%	51%	53%	58%	47%
Best focus (mm)	13	10	10	8	8	10
Depth of focus	5 - 40	3.5 - 50	3 - 50	4 - 40	3 - 50	4 - 50
Module Size (mm)	1x1x1.69 2.2x1x1.69(2)	1x1x1.72	1x1x1.74	1x1x1.48	1x1x1.43	1x1x1.40

(1) 2x for NanEye Stereo.

(2) For NanEye Stereo.

6 Typical Operating Characteristics

Figure 13:
B&W Spectral Response

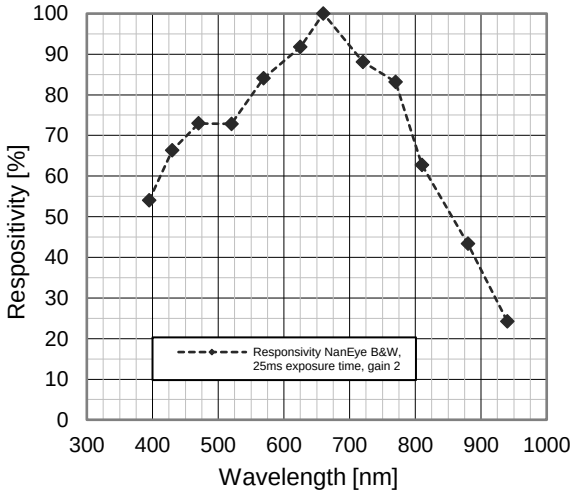


Figure 14:
RGB Spectral Response

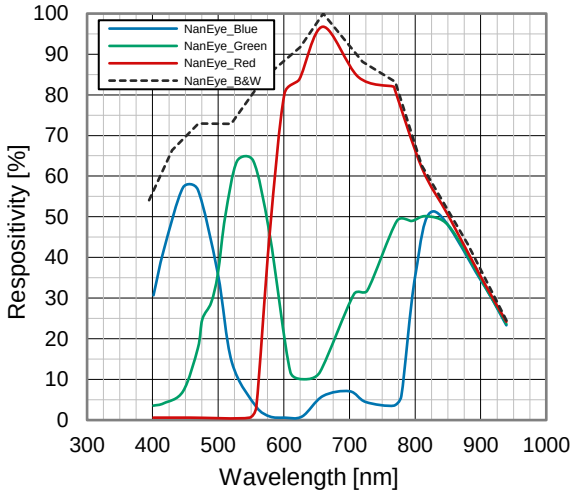


Figure 15:
Frame Rate vs Voltage(1)(2)

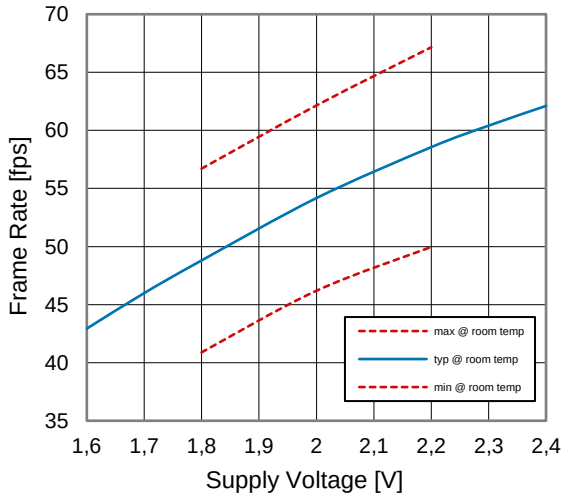
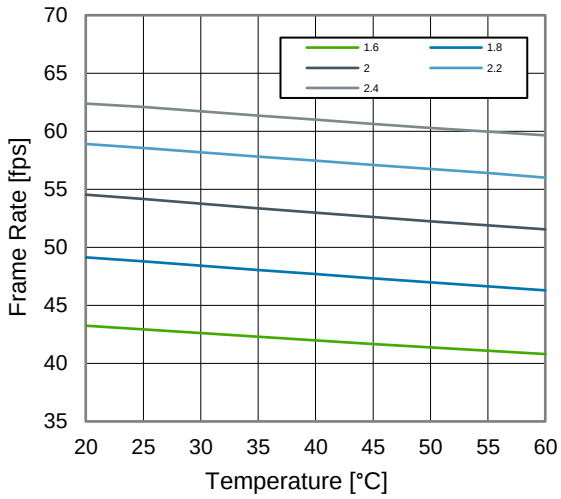
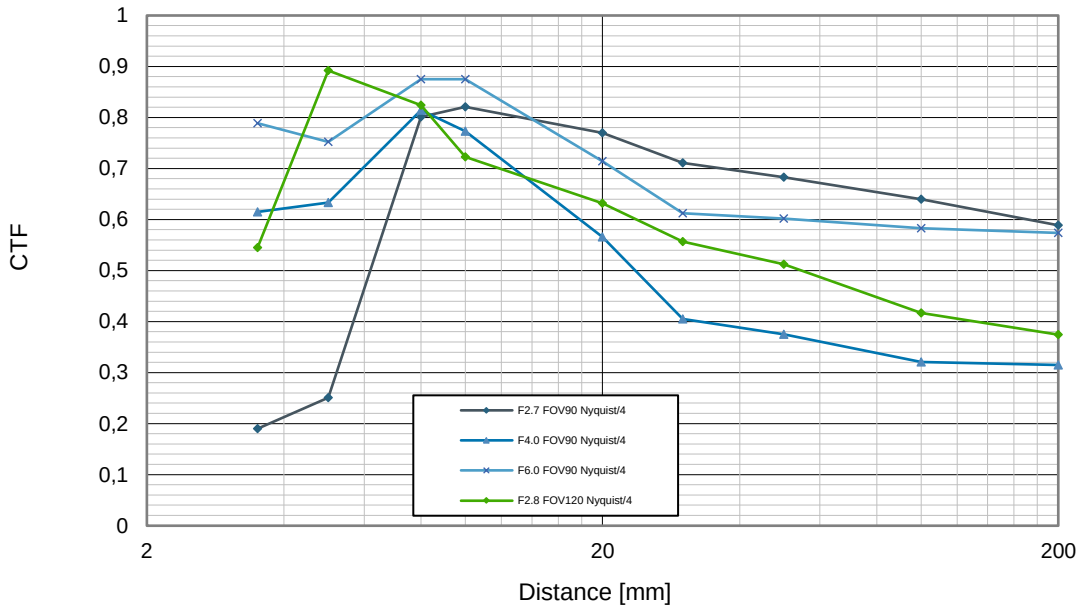


Figure 16:
Frame Rate vs Temperature(2)



(1) Min/max values based on current available test results, limits may be adjusted when additional test data are available.
(2) The frame rate is dependent on VDD sensor supply voltage. For as long as the frame rate is maintained >38 Fps the sensor supply can be set lower than 1.8V down to 1.6V minimum.

Figure 17:
NanEye CTF Measurements



7 Functional Description

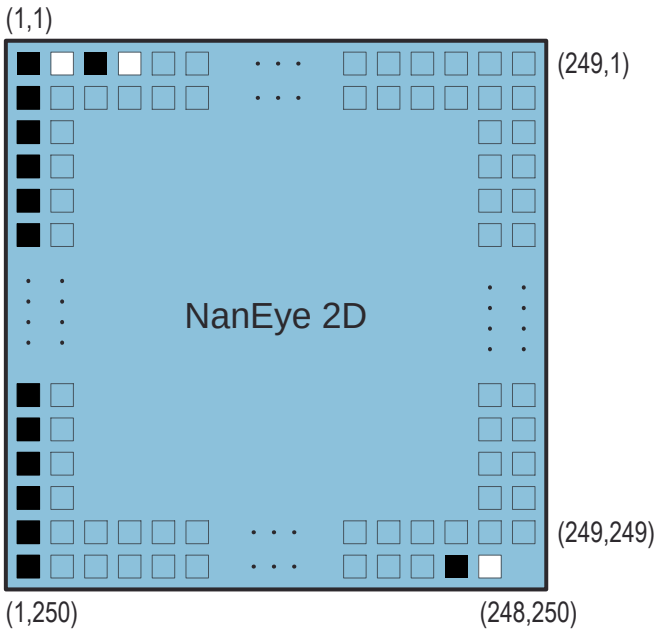
7.1 Sensor Architecture

Figure 2 shows the image sensor architecture. The internal state machine generates the necessary signals for image acquisition. The image is stored in the pixels (rolling shutter) and is read out sequentially, row-by-row. On the pixel output, an analog gain is possible. The pixel values then passes to a column ADC cell, in which ADC conversion is performed. The digital signals are then read out over a LVDS channel.

7.1.1 Pixel Array

The pixel array consists of 249 x 250 square rolling shutter pixels with a pitch of 3µm (3µm x 3µm). This results in an optical area of 747µm x 750µm (1.06mm diameter).

Figure 18:
Pixel Array



The pixels are designed to achieve maximum sensitivity with low noise.

There are two electrical black pixels and two electrically saturated pixels on the upper left corner and one black pixel and one white pixel on the lower right corner, which may be used to check consistency of received data.

7.1.2 Analog Front End

The analog front end consists of 2 major parts, a column amplifier block and a column ADC block.

The column amplifier prepares the pixel signal for the column ADC. The column ADC converts the analog pixel value to a 10 bit value and can apply a gain. All gain and offset settings can be programmed using the I2C interface.

7.1.3 LVDS Block

The LVDS block converts the digital data coming from the column ADC into standard serial LVDS data running at around 30 Mbps. During transfer of the image data, the pixel values are transmitted in bit serial manner with 12 bits and embedded clock (start bit (1bit) + data (10bits) + stop bit (1bit)). The sensor has one LVDS output pair.

7.1.4 State Machine

The state machine will generate all required control signals to operate the sensor. The clock is derived from an on-chip master clock generator running at about 2.5MHz. This sequencer can be programmed through the I2C interface. A detailed description of the registers and sensor programming can be found in section 7.5 and 8 of this document.

7.1.5 Single Ended Serial Interface

The single ended serial interface is used to load the register with data. It is multiplexed with the LVDS interface, data can be send in the frame windows of the receiving image information. The data in these register is used by the state machine and ADC block while driving and reading out the image sensor. Features like exposure time, gain and offset can be programmed using this interface. Section 7.5 and 8 contain more details on register programming.

7.1.6 Optics

The optional optics available for the sensor is a high performance miniature lens module. It will be directly mounted on the image sensor and has its best focus position defined by design, so no mechanical set of focus is needed. The material is based on B33 (Borofloat glass). The design is made in such way that the surface towards the object is flat, so the lens performance is not influenced by the medium between the object and lens. Only the opening angle of the lens is reduced when the system operates in water.

7.2 Driving the NanEye / NanEye Stereo

The NanEye / NanEye Stereo image sensor is a CMOS based system on chip, which means that no external component close to the sensor is needed to run the sensor, not even an external capacitor.

7.2.1 Supply Voltage

The sensor operates from a single supply voltage VDDD. All blocks are supplied by this voltage. In addition a VDDPIX (reset voltage for the pixels) is generated internally.

For reference schematic and external components please refer to section 9.

7.2.2 Start-Up Sequence

The chip is fully self-timed. After power on, the sensor performs an internal power on reset, and then starts autonomous operation and transmission of image data in rolling shutter mode, using maximum exposure time.

7.2.3 Reset Sequence

No special reset sequence needed.

7.2.4 Frame Rate

If required, the sensor data rate can be modulated slightly by adjusting the sensor supply voltage (see Figure 15 and Figure 16). If multiple sensors are to be synchronized, this is possible by dynamically adjust the supply voltage to control the frame rate.

7.3 Matrix Readout

After power on the sensor starts to loop autonomously the sequence as detailed below:

Figure 19:
Sequence of Operation Graph

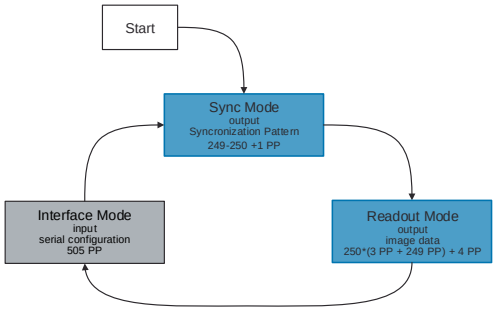


Figure 20:
Sequence of Operation

Phase #	Status	Start Bit	Data XOR	Interface Status	Duration	Function
1.1	Transmission of continuous 0	0	Yes	LVDS out	3 PP(1)	Row 1 Readout
1.2	Transmission of 249 pixel values (first pixel is black)	1	Yes	LVDS out	249 PP	
2.1	Transmission of continuous 0	0	Yes	LVDS out	3 PP	Row 2 Readout
2.2	Transmission of 249 pixel values (first pixel is black)	1	Yes	LVDS out	249 PP	
Readout of all 250 rows, repeat x.1 and x.2 consecutively						
250.1	Transmission of continuous 0	0	Yes	LVDS out	3 PP	Row 250 Readout
250.2	Transmission of 248 pixel values (first pixel is black)	1	Yes	LVDS out	248 PP	
251	Transmission of continuous 0	0	No	LVDS out	4 PP	Indication for end of frame
252	Time for Serial configuration(2)	--	--	Serial configuration input	505 PP	Register configuration
253	Transmission of synchronization pattern before start of frame, continuous 0	0	Yes	LVDS out	249 - 250 PP	Resynchronization with sensor data & pixel clock
253a	At the end of the synchronization pattern, a random bit sequence (can be all 0) is transmitted while switching to the first start of line identification.	X	Yes	Change to readout state	1 PP	Change of state; do filter this word and ignore it.
Restart at 1.1						

(1) PP = Pixel Period
(2) It is recommended to drive the data bus during the entire upstream communication phase, even if no register data is sent to the sensor. This is to avoid pick up of EMI on the non driven lines floating during the communication.

CAUTION

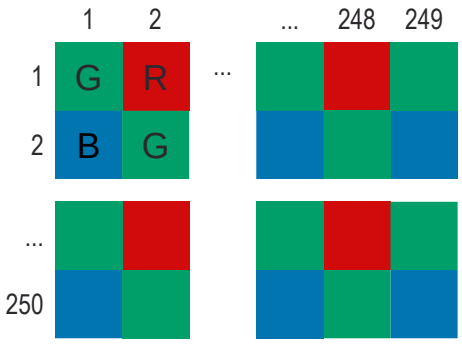
The sensor fully self timed and cycles between the downstream and the upstream mode. Therefore, it is the user's responsibility to tristate the upstream drivers of the serial configuration link prior to the start of data transmission from the sensor. If the bus is still driven by the upstream configuration buffers when the sensors starts down stream of the first pixels information, these may not be captured correctly.

Due to the limited current output from the sensor it is not expected that conflicting drive of the data lines will permanently destroy the sensor, however this condition would seriously degrade the data integrity and is not qualified in terms of device reliability and life time.

7.3.1 Color Filters

When a color version of the NanEye / NanEye Stereo is used, the color filters are applied in a Bayer pattern. The first pixel read-out, pixel (1,1), is the top left ion and has a green filter.

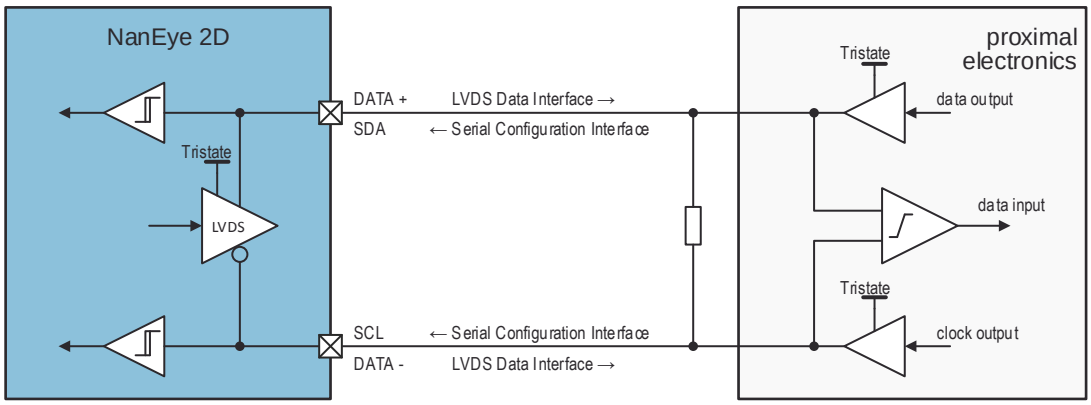
Figure 21:
Colored Version Bayer Pattern Matrix



7.4 Serial Interface

The chip features a bi directional data interface. During transfer of the image data, the pixel values are transmitted in bit serial manner over an LVDS channel with an embedded clock. After each frame, the data interface is switched for a defined time to an upstream configuration interface. This needs a synchronization every time it passes from the upstream to a new downstream mode at the image receiver side. The positive LVDS channel holds the serial configuration data and the negative channel holds the serial interface clock.

Figure 22:
Data Interface between Sensor and Proximal Electronics



7.4.1 LVDS Data Interface (Downstream)

The NanEye_2D chip works with an on chip clock of ~2.5MHz. The image data on chip is generated as a 10-bit representation. A start and a stop bit is then added to the data. The bit serial data interface then transmits the data at 12 x 2.5MHz bit rate (+/- 20%), ~ 30MHz.

Data Word

The data word is EXOR gated with the serial clock before sent bit serial according to the following scheme:

Figure 23:
Data Word Encoding

Bit #	0	1	2	3	4	5	6	7	8	9	10	11
Function	Start	Pixel Data (10 bits)										Stop
Content	1	MSB									LSB	0

An example of this is:

- 10bits data word: 0110001101
- Including start and stop bits: **1**01100011010**0**
- 12bits word EXOR with the data clock:
  - 10 10 10 10 10 10 10 10 10 10 10 10 - data clock (main clock)
  - 11 00 11 11 00 00 00 11 11 00 11 00 - 12 bit data @ data clock frequency
  - 01 10 01 01 10 10 10 01 01 10 01 10 - data word result

Start of Row

The start of a line identification consists in 3x sending the word 00 with start and stop bits also at 0.

Figure 24:
Start of Line Word Encoding

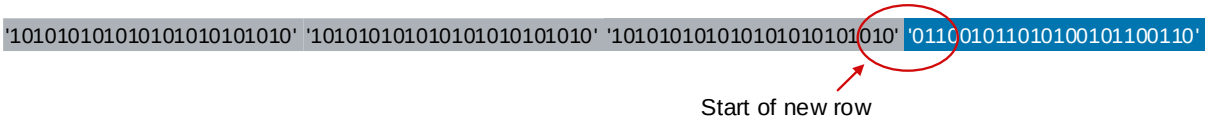
Bit #	0	1	2	3	4	5	6	7	8	9	10	11
Function	Start	Start Row										Stop
content	**0**	0	0	0	0	0	0	0	0	0	0	0

An example of this is:

- 10bits data word: 0000000000
- Including start and stop bits: **0**00000000000
- 12bits word EXOR with the data clock:
  - 10 10 10 10 10 10 10 10 10 10 10 10 - data clock (main clock)
  - 00 00 00 00 00 00 00 00 00 00 00 00 - 12 bit at 0's @ data clock frequency
  - 10 10 10 10 10 10 10 10 10 10 10 10 - start of line word result

The resulting start word is sent 3x at the start of a new row. The beginning of a new row can be easily identified by the detection of the first start bit:

Figure 25:
Start of Row Identification



7.4.2 Serial Configuration Interface (Upstream)

The upstream data interface consists of a single 16 bit write only register. The register is written by sending a 4 bit update code, followed by a 3 bit register address (only register 00 is implemented) and 16bit register data.

Maximum frequency of SCL can be 2.5MHz.

All data is written MSB to LSB. Data is captured on the rising edge of SCL. It is recommended to change SDA on the falling edge of SCL to grant maximum setup and hold times.

The below table indicates the sequence of writing update code, register address and register data.

Figure 26:
Register Update Sequence

# rising edge of SCL after reset	1	2	3	4	5	6	7	8	9	…	22	23	24
Function	update code				register address			register content (16 bit)					reset
Content	1	0	0	1	**0**	**0**	**0**	MSB				LSB	

The content of the input shift register is updated to the effective register, once a correct update code (1001) has been received and shifted by 24 clocks. The input shift register is reset to all 0's 24 clocks after the first high value as the SDA input is received, regardless of whether a correct update code is detected or not.

7.5 Sensor Programming

This section explains how the NanEye / NanEye Stereo can be programmed using the on-board registers.

7.5.1 Exposure Time Control

Exposure time is defined based on the amount of rows in reset, set by user. The NanEye / NanEye Stereo sensor feature a rolling shutter, which means one row is selected for readout while a defined number of previous rows are in reset, and all the others rows are in integration. The range goes from [0 - 248] lines. The default value is 1 "Nrows_in_Reset = 00000001".

The effective exposure time thus is given by the formula:

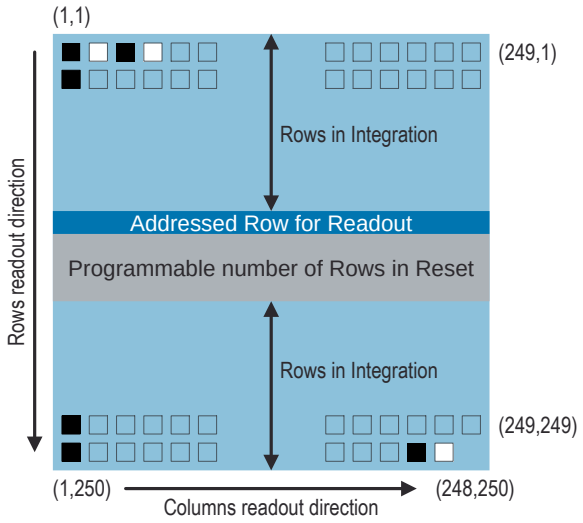
Equation 1:

$$T_{exp} = \frac{max[N_{rows} - N_{RowsInReset}; 2]}{N_{rows}} \times F_{time}$$

Where:

T_{exp} = The effective exposure time
N_{rows} = 250
$N_{RowsInReset}$ = register setting *rows_in_reset* [0 …248]
F_{time} = The time for a frame readout (22.7ms for NanEye 2D @ VDD = 2.1V)

Figure 27:
Row Readout Operation



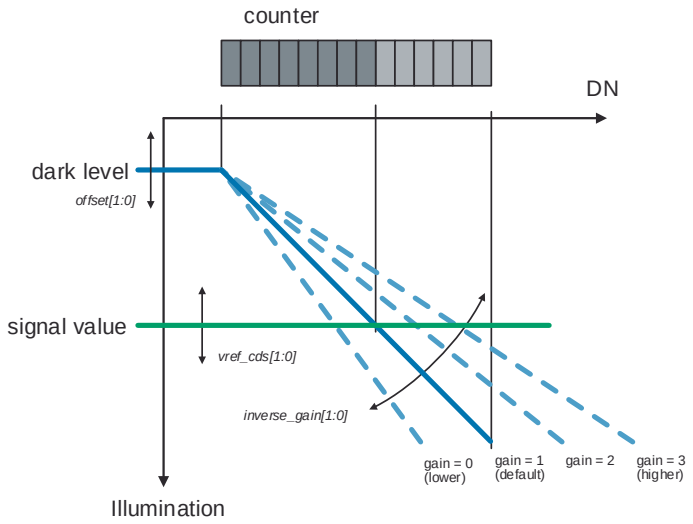
7.5.2 Offset and Analog Gain

It is a 10bits full linear ADC. The architecture of the ADC allows to program several items:

- Voltage Reference for signal (*vref_cds[1:0]*)
- Ramp Gain (*inverse_gain[1:0]*)
- Ramp Offset Voltage (*offset[1:0]*)

See the configurable values in section 8 Register Description.

Figure 28:
ADC Settings



8 Register Description

8.1 Detailed Register Description

Figure 29:
Configuration Register

Addr: 00h		Configuration		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
15:14	VREF_CDS[1:0]	10b	WO	Sets CDS reference voltage: 0: 1.3V 1: 1.4V **2: 1.5V (recommended)** 3: 1.6V
13:12	VRST_PIXEL[1:0]	10b	WO	Sets pixel reset voltage: 0: 1.2V 1: 1.3V (recommended) **2: 1.4V** (do not use)(1) 3: 1.5V (do not use)
11:10	OFFSET[1:0]	01b	WO	Sets ADC ramp offset (dark level): 0: Low **1: Default** 2: Mid 3: High
8:9	INVERSE_GAIN[1:0]	10b	WO	Sets inverse ADC ramp gain: 0: Gain = 3 1: Gain = 2 **2: Gain = 1** 3: Gain = 0
7:0	ROWS_IN_RESET[7:0]	01h	WO	Sets number of rows in reset (exposure time): 0: 0 rows **1: 1 row** 2: 2 rows … 248: 248 rows 249: do not use … 255: do not use

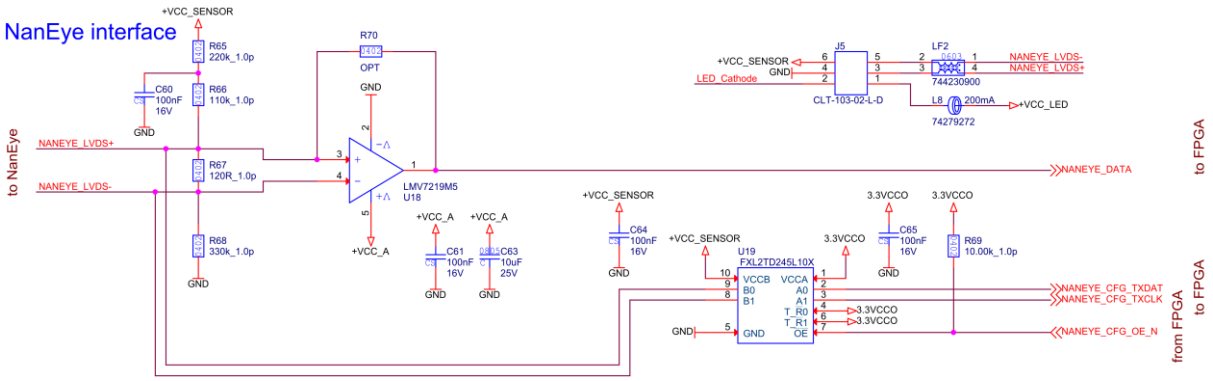
(1) It is recommended to set VRST_PIXEL[1:0] to 01b (1.3V) direct after startup of the sensor.

9 Application Information

9.1 Recommended LVDS Receiver Electronics

The direct interface of the LVDS data to an FPGA or DSP differential input is not guaranteed. It is recommended to use a LVDS detections circuit based on a fast comparator, which fixes the LVDS signals common mode.

Figure 30:
NanEye Interface Schematic (for information only)



In order to increase the robustness of the de serialization under the presence of significant jitter which should be expected from the on chip oscillator, the data is EXOR combined with the data clock.

To reliably de serialize the incoming data, the receiver side should sample the data at least with 300MHz to properly detect the phase of the transitions.

When defining the drive strength of the up stream drivers in the proximal circuitry it has to be considered that the serial clock and the serial data will couple to each other over the bit lines termination resistor.

Driving the serial configuration data should be carefully designed along with the cables inductance to avoid signal over shoot at the chip side. It is recommended to use slew rate controlled drivers with a low slew rate. No distal termination of the data lines is implemented on chip.

CAUTION

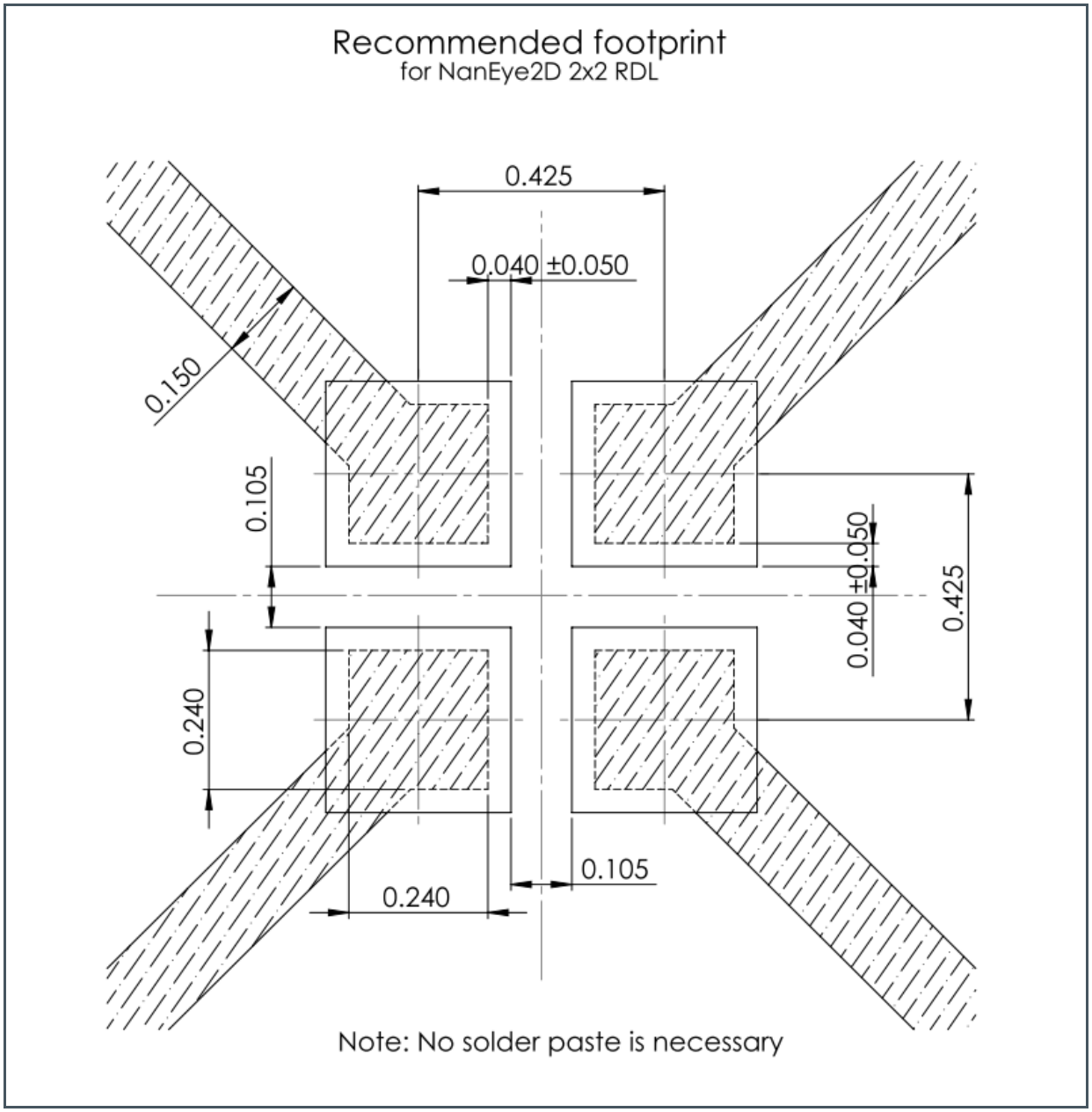
The PCB connector may short VDDD and LED+ inside the socket during insertion or removal. Switch off the LED supply before plugging in/out the PCB connector or use appropriate protection

9.2 Application Notes

It is possible to correct the “reset line” artefact. Please refer to the application note “NanEye_NanEyeStereo_AN000447”.

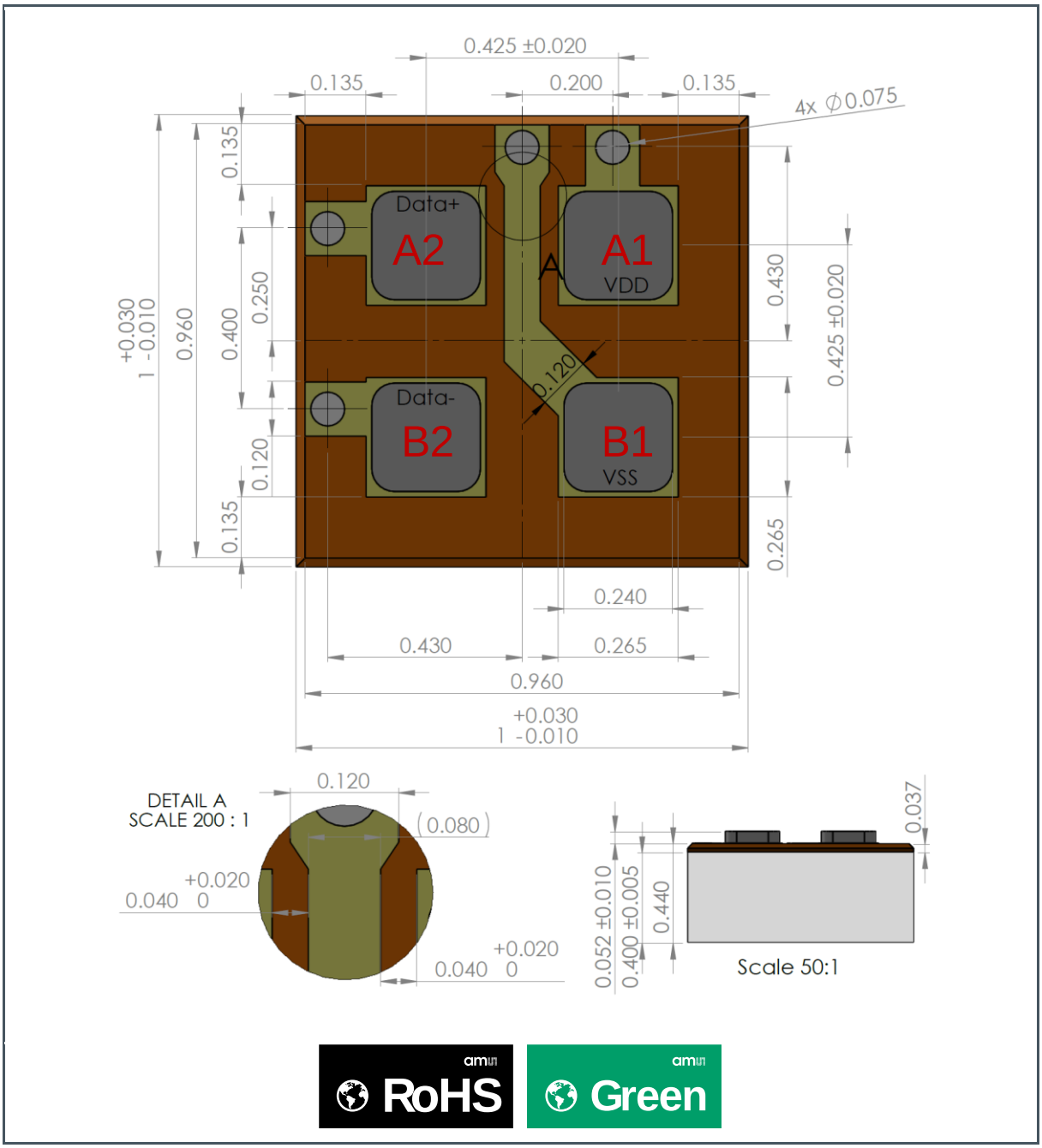
9.3 PCB Layout

Figure 31:
SGA 2x2 Footprint and Layout



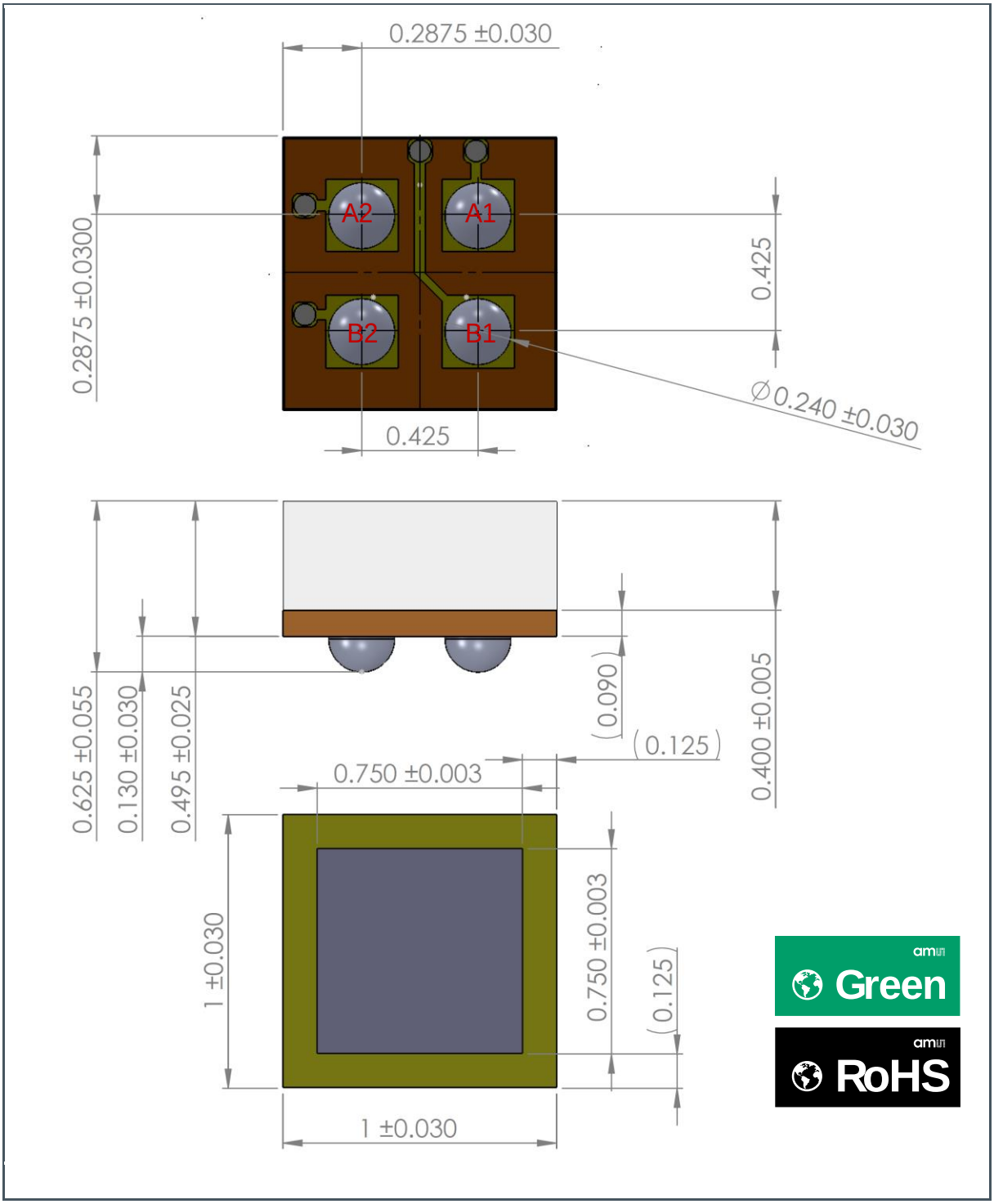
10 Package Drawings & Markings

Figure 32:
SGA 2x2 Package Outline Drawing Square Contacts (bottom view)



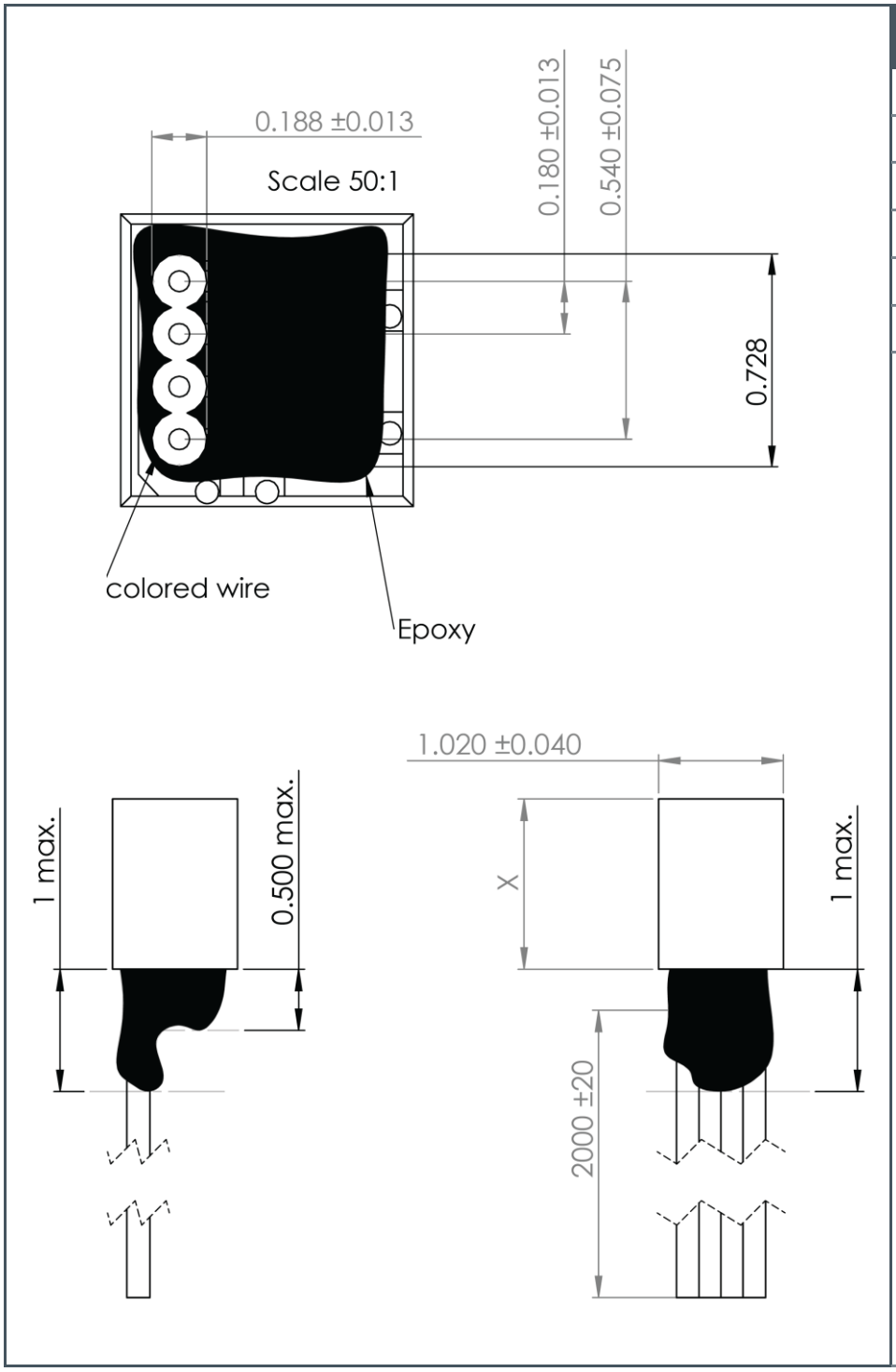
(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are +/-0.04mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

Figure 33:
SGA 2x2 Package Outline Drawing Round Contacts (bottom view)



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are +/-0.04mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

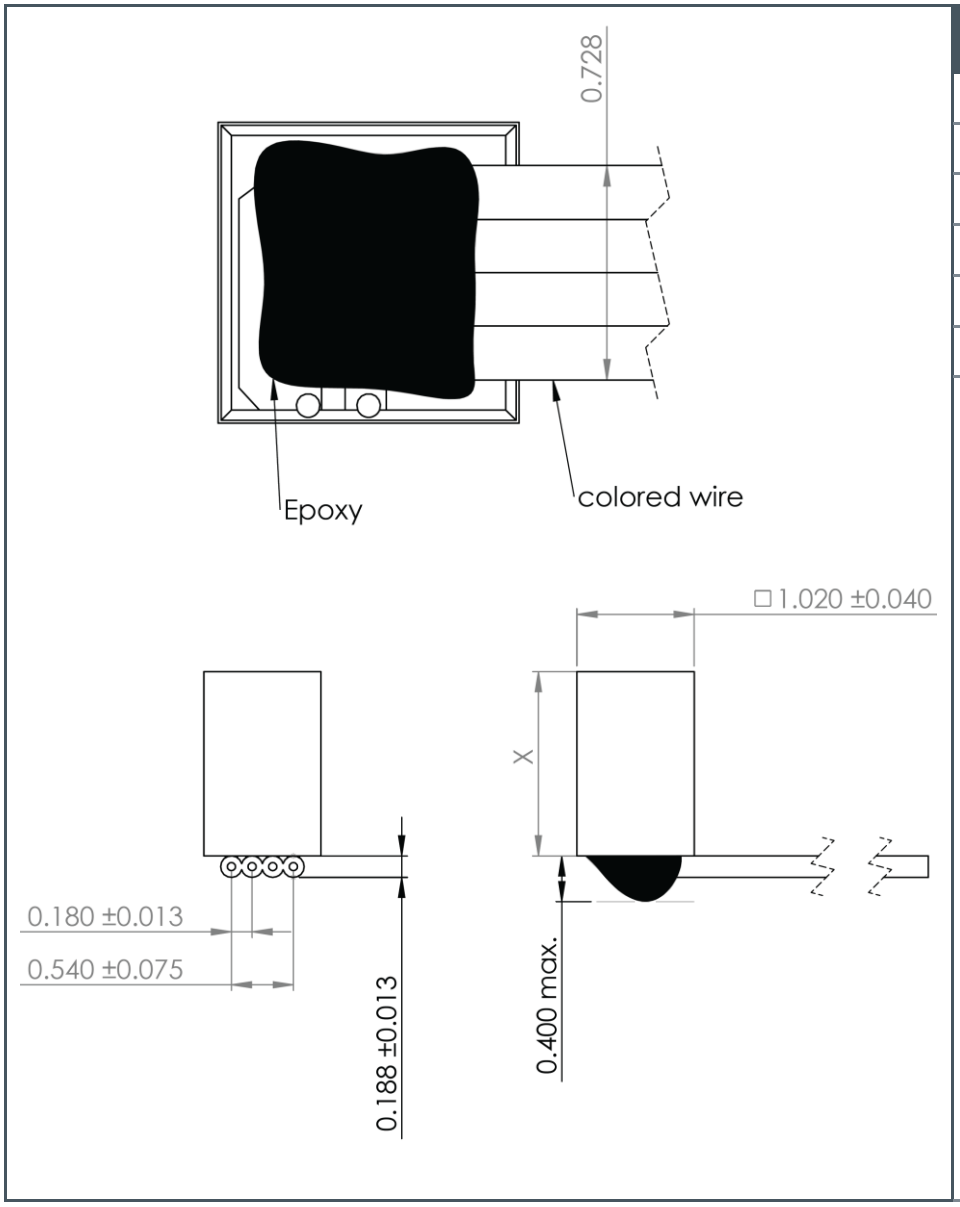
Figure 34:
NanEye with Lens and Cable Soldered Dipped (Bended) Package Outline Drawing



Lens	X
F2.7 FOV 90°	1.63
F4.0 FOV 90°	1.66
F6.0 FOV 90°	1.68
F2.8 FOV 120°	1.42
F4.0 FOV 120°	1.46
F2.4 FOV 160°	1.34

(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are +/-0.1mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

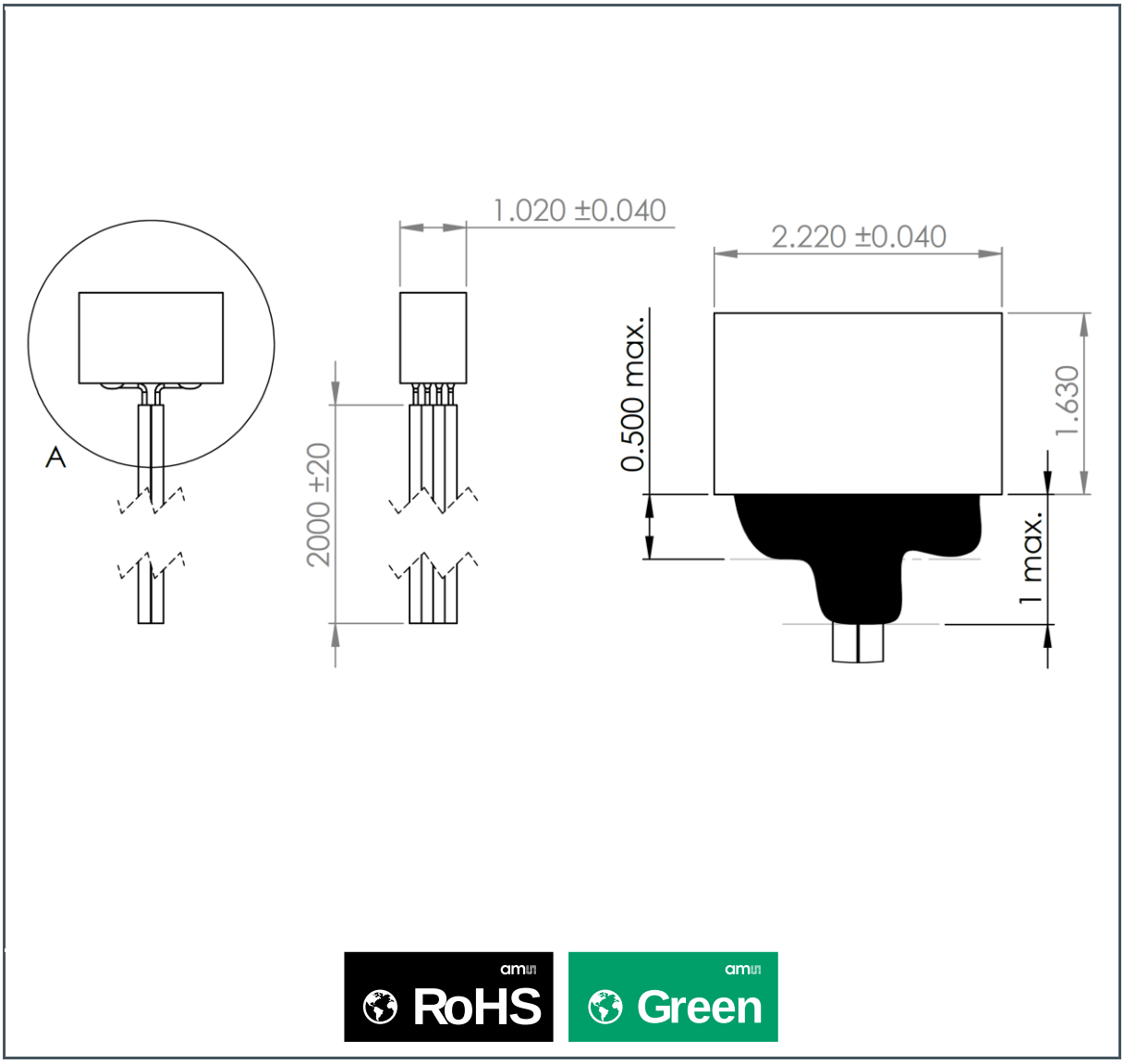
Figure 35:
NanEye with Lens and Cable Soldered Dipped (90°) Package Outline Drawing



Lens	X
F2.7 FOV 90°	1.63
F4.0 FOV 90°	1.66
F6.0 FOV 90°	1.68
F2.8 FOV 120°	1.42
F4.0 FOV 120°	1.46
F2.4 FOV 160°	1.34

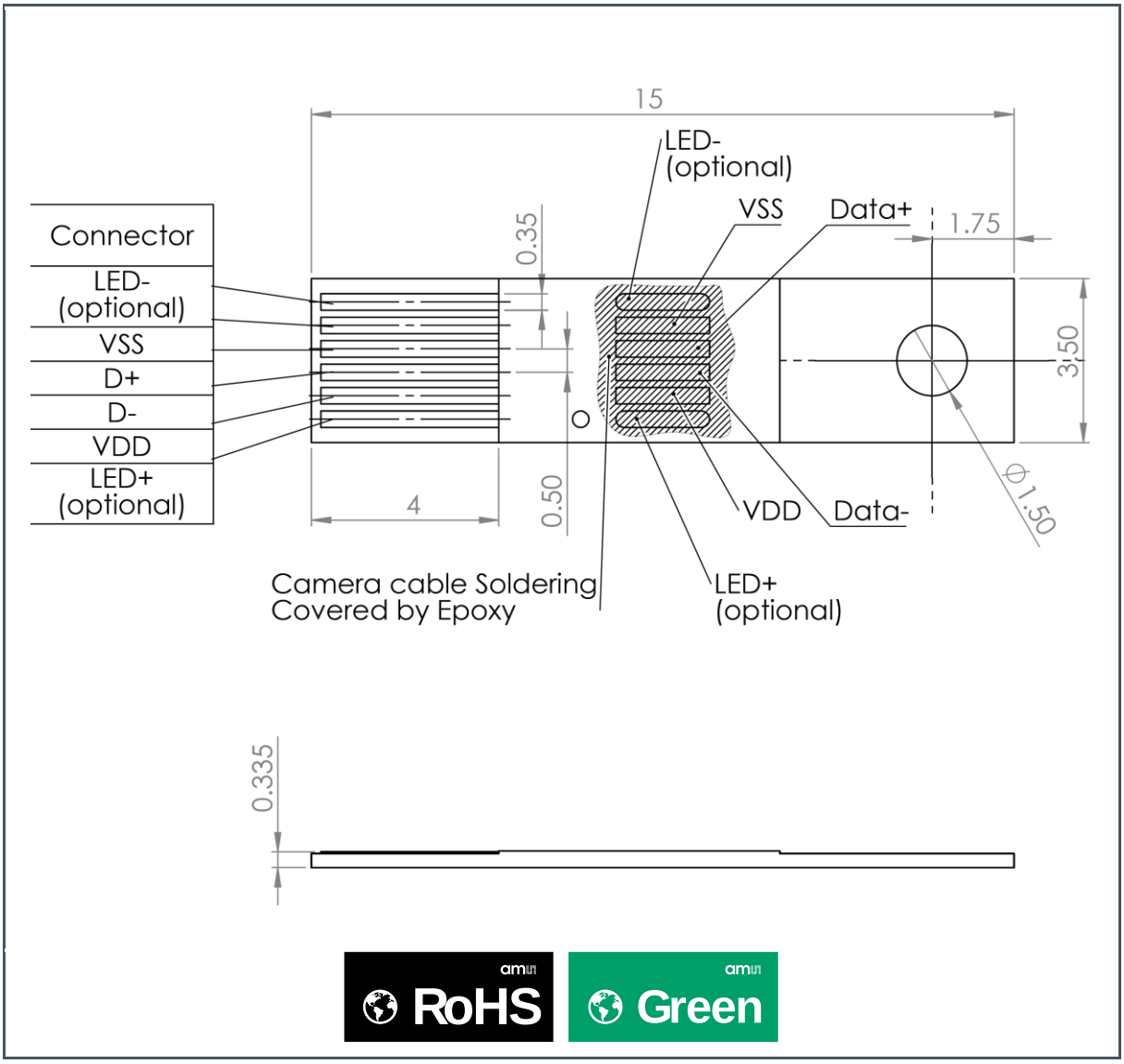
(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are +/-0.1mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

Figure 36:
NanEye Stereo Package Outline Drawing



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are +/-0.1mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

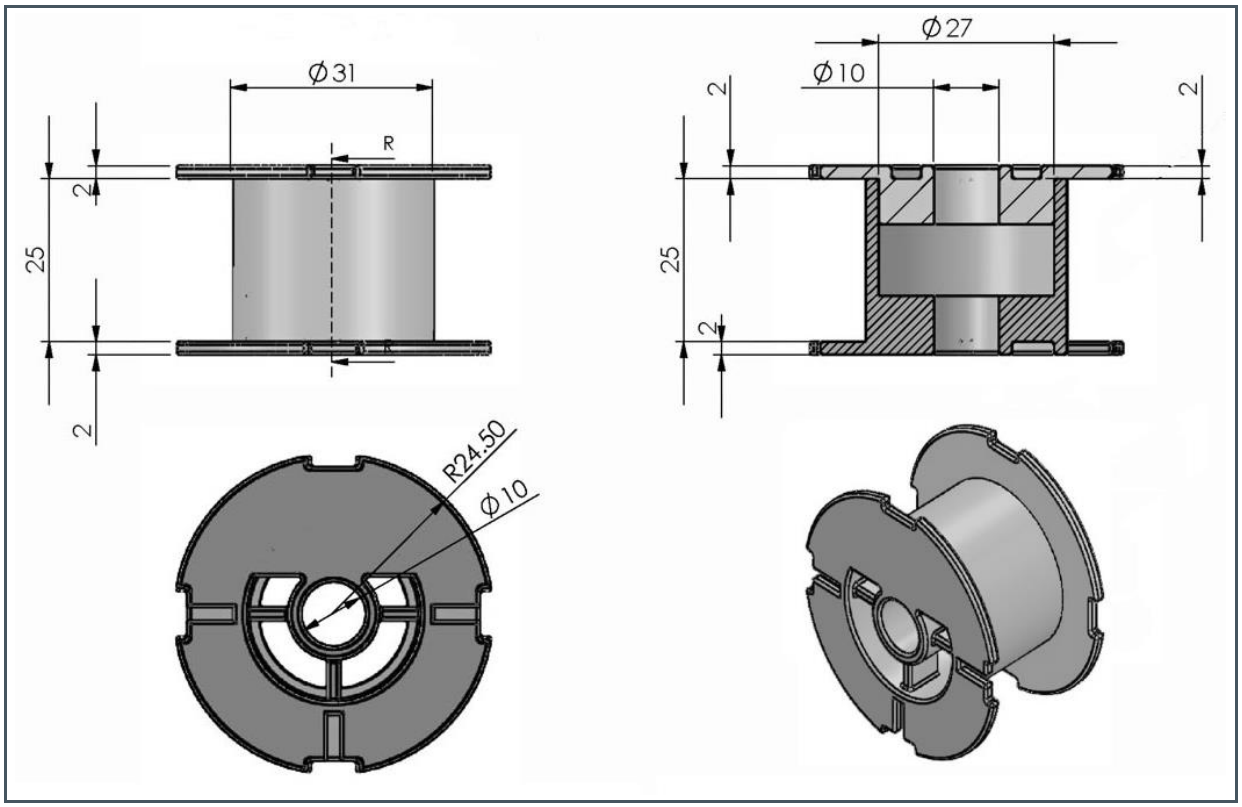
Figure 37:
FlexPCB Connector Outline Drawing



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are +/-0.1mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

11 Tape & Reel Information

Figure 38:
Spool Dimensions for Module plus Cable Shipments



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are +/-0.1mm.
(3) This drawing is subject to change without notice.

12 Chemical Composition

Figure 39:
Chemical Composition with Lens

Chemical Element/Material	Percentage of Component Mass(3)
SiO_2	64.49%
B_2O_3	10.35%
Na_2 / K_20	3.18%
Al_2O_3	1.59%
Si	13.70%
Cu	0.81%
Sn	1.39%
Organic Polymers	4.48%

(1) Approx. weight with lens and no side wall coating: 2200µg.

Figure 40:
Chemical Composition without Lens

Chemical Element/Material	Percentage of Component Mass(3)
SiO_2	67.58%
B_2O_3	10.85%
Na_2 / K_20	3.34%
Al_2O_3	1.67%
Si	8.84%
Cu	1.69%
Sn	2.91%
Organic Polymers	3.13%

(1) Approx.. weight without lens: 1050µg
(2) All values are approximate indication only, based on per-design material breakdown and indications of our suppliers. **ams** does not perform material composition analysis. Percentages may not total 100 due to rounding.

13 Appendix

13.1 Evaluation System

Optionally with the NanEye / NanEye Stereo Module, **ams** provides a base station and software to run the device on a PC in real-time with all necessary image corrections. The complete system consists of the module, the USB base station and the PC software.

14 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Changes in revision v2-02	
Changed storage conditions, Table reorganized	9
Changed Ordering Codes	5,6
Corrected Data Word and Start of row encoding	20,21
Changes in revision v2-01	
Corrected packing method for modules without cable	5
Corrected available standard camera modules	5
Corrected drawing for stereo camera module	31
Changes in revision v2-00	
Added MSL level package footnote	9
Corrected LVDS bit speed	11
Corrected MTF and Best Focus values	13
Corrected x-axis to [mm] for CTF diagram	14
Added Chapter “7.1.6 Optics”	16
Added recommended values for VRST_PIXEL and VREF_CDS	25

Changes from previous version to current revision v2-02	Page
Added additional SGA footprint	28
Changed document type from CONFIDENTIAL to PUBLIC	all

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

15 Legal Information

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